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Design and Implementation of a Low-Power Transmitter for Medical Applications

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Abstract

Wireless Sensor Networks (WSNs) have become increasingly important in biomedical applications, where the FCC allocates the MICS bandwidth specifically for medical sensor devices. These networks enable sensor nodes to collect vital signals such as ECG, EEG, EMG, blood pressure, body temperature, and heart rate and transmit the data to a base station for storage, processing, and monitoring. The widespread adoption of Radio Frequency (RF) communications has significantly influenced modern healthcare technologies, encouraging research and investment from academia and industry. RF-based systems provide the advantage of wireless data transfer, which reduces wiring complexity and enhances flexibility in medical devices. For reliable communication, both transmitters and receivers must comply with specific operational parameters to minimize interference and ensure accurate data transmission. This study focuses on the design of a low-power transmitter for medical sensor applications, emphasizing efficient bandwidth usage, minimal energy consumption, and compatibility with sensor nodes. The proposed design aims to improve the performance of wireless medical monitoring systems and facilitate real-time data collection and analysis.

Keywords: Transmitter design, Medical applications, Low-power, Bandwidth, Sensor node.

1 | Introduction

Wireless Biomedical Sensor Networks (WBSNs) have rapidly evolved into a key enabling technology for continuous and real-time health monitoring. These systems allow long-term observation of physiological signals such as Electrocardiogram (ECG), Electroencephalogram (EEG), Electromyogram (EMG), blood pressure, respiration rate, and body temperature [1], [2]. By enabling remote diagnostics and early detection of abnormalities, WBSNs significantly reduce hospitalization costs and improve patient quality of life, particularly for elderly and chronically ill populations. To support reliable short-range communication for implantable and wearable medical devices, the Federal Communications Commission (FCC) has allocated the Medical Implant Communication Service (MICS) band (402-405 MHz) specifically for biomedical telemetry systems [3], [4]. Operation in this band offers controlled interference conditions and regulated transmission power, ensuring safe and stable communication for medical applications. However, stringent spectral masks

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and severe power constraints imposed on MICS-band devices present substantial challenges in RF circuit design. In biomedical sensor nodes, ultra-low energy consumption is the dominant design requirement due to limited battery capacity and the impracticality of battery replacement in implantable devices. Among all subsystems, the RF transmitter typically dominates overall power consumption, making it the primary bottleneck in extending system lifetime [5]. Therefore, developing energy-efficient transmitter architectures is essential for sustainable biomedical monitoring systems. Conventional MICS-band transmitters frequently employ Phase-Locked Loop (PLL) based frequency synthesizers to achieve carrier stability and spectral compliance [6–8]. Although PLL architectures provide accurate frequency generation and flexible modulation, they introduce significant drawbacks, including high static and dynamic power consumption, increased silicon area, longer startup time, and design complexity. For low-data-rate biomedical signals, the overhead associated with PLL-based architectures is often disproportionate to system requirements [9]. Injection-Locked Oscillators (ILOs) have emerged as an attractive low-power alternative for frequency stabilization. By exploiting synchronization phenomena, ILOs enable frequency control with significantly reduced complexity and energy consumption. Additionally, harmonic injection techniques allow frequency multiplication without requiring high-frequency oscillators at early stages, thereby reducing switching activity and dynamic power, which scales proportionally with operating frequency. Despite the advantages of injection-locked architectures, existing designs often rely on partial PLL assistance, direct high-frequency modulation, or limited harmonic exploitation [10], [11]. Many previously reported biomedical transmitters either maintain PLL blocks for frequency accuracy or perform modulation directly at carrier frequency, leading to increased power consumption. Furthermore, harmonic locking strategies have rarely been combined with distributed frequency multiplication across multiple circuit stages to optimize energy efficiency [12]. Consequently, there remains a need for a fully PLL-free transmitter architecture that:

I. Performs modulation at significantly reduced reference frequency.

II. Utilizes harmonic injection locking for stable carrier generation.

III. Integrates frequency multiplication within the power amplification stage to minimize overall dynamic power consumption.

In this work, a novel 408-MHz PLL-free BFSK transmitter for biomedical sensor applications is proposed. The architecture performs modulation at a reference frequency 13 times lower than the carrier frequency, substantially reducing switching losses. A three-stage ring oscillator is injection-locked to the fourth harmonic of the reference signal, while triple frequency multiplication is embedded in the power amplifier stage. This distributed frequency scaling strategy eliminates the need for a conventional PLL while preserving spectral integrity and fast settling characteristics. The proposed design targets ultra-low-power wearable and implantable biomedical systems operating within the MICS band [13]. The remainder of this paper is organized as follows. Section II describes the overall transmitter architecture and operational principle. Section III details the injection-locked ring oscillator and harmonic locking mechanism. Section IV presents circuit-level implementation and simulation results, including phase noise and spectral analysis. Section V provides a comparative evaluation with previously reported medical transmitters. Finally, Section VI concludes the paper and outlines future research directions [14], [15].

2 | Methodology

This research presents the design and implementation of an ultra-low-power transmitter compliant with the MICS standard for implantable biomedical devices. In order to minimize overall power consumption and circuit complexity, conventional mixer and power amplifier blocks are intentionally omitted. Consequently, the transmitter architecture is fundamentally centered on the design of a low-phase-noise oscillator, which serves as the core RF signal generation unit [16]. To enhance spectral purity while maintaining low power operation, an N-path filter-based oscillator topology is proposed as an alternative to the conventional LC-tank oscillator [17]. Unlike LC-based structures, the proposed architecture eliminates the need for on-chip inductors, thereby reducing silicon area and mitigating process-induced variability. Moreover, frequency

tuning is achieved through path switching mechanisms rather than varactor-based capacitance variation, resulting in improved linearity and enhanced frequency agility. For performance validation, both the proposed N-path oscillator and a conventional LC oscillator are designed and simulated using TSMC 0.18 μm CMOS technology. A comparative analysis is conducted in terms of phase noise, power consumption, frequency stability, and tunability. All schematic-level simulations, harmonic balance analyses, and phase-noise characterizations are performed in Advanced Design System (ADS) to ensure accurate RF modeling and spectral evaluation. Following oscillator optimization, the complete transmitter architecture is integrated and evaluated against MICS regulatory requirements [17]. Key performance metrics, including total power consumption, output spectrum purity, and compliance with adjacent channel interference constraints, are systematically analyzed. The overall research methodology is structured into sequential stages: 1) extraction of MICS RF specifications, 2) oscillator topology design and optimization, 3) transmitter-level integration, and 4) comprehensive RF performance validation

2.1 | Circuit Architecture and Design Strategy

To evaluate the effectiveness of the proposed low-power adaptive amplifier, the circuit was implemented in CMOS technology and analyzed under two different process nodes: 0.18 μm and 90 nm. The design objective was to achieve high stability, low power consumption, and acceptable Slew Rate (SR) performance for biomedical implantable applications. The amplifier consists of two main functional blocks as shown in *Fig. 1*:

I. Core two-stage amplifier

II. Adaptive Biasing Current Circuit (ABCC)

The ABCC block dynamically adjusts the bias current of the differential pair based on output variations. This adaptive mechanism improves transient response and stability without permanently increasing static power consumption. The ABCC is composed of three subcircuits:

I. Current Monitor Circuit (CMC)

II. Current Comparison Circuit (CCC)

III. Current Amplification Circuit (CAC)

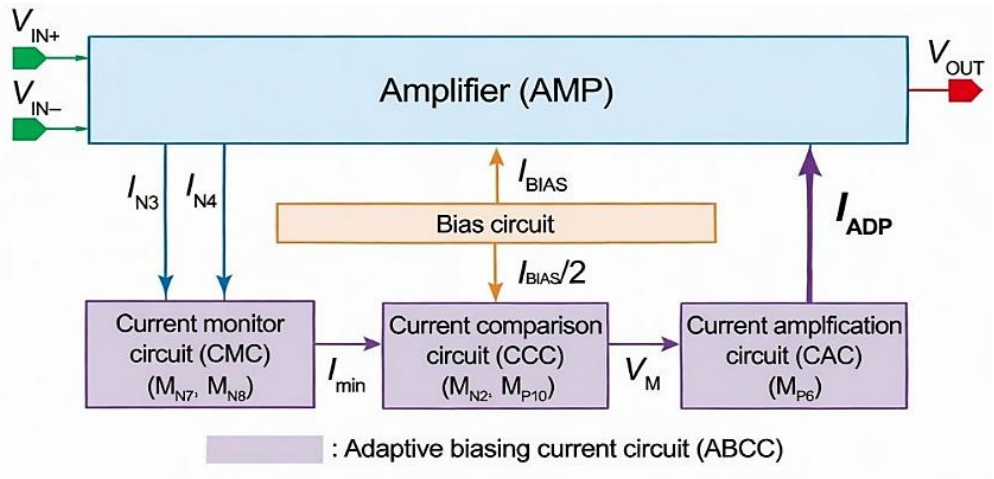

Fig. 1. Circuit schematic.

The CMC extracts a small branch current from the differential pair using matched transistor gate voltages. Since the source voltage of the input pair transistors is approximately zero, the drain current is primarily governed by V_{GS}, enabling accurate current sensing. The CCC performs current mirroring and scaling as *Eqs. (1)-(4):*

$$\mathrm{ID(MN2)} = ½ \times \mathrm{ID(MN1)}. \quad (1)$$

$$\mathrm{ID(MN1)} = \mathrm{IBias}. \quad (2)$$

$$ID(MN2) = ½ \times IBias. \quad (3)$$

$$½ \times IBias = Imin. \quad (4)$$

The current difference between branches is converted into a control voltage V_m via compensation capacitor C_{C1}. This voltage drives the CAC block, implemented using transistor MP6, which functions as an adaptive current source. When transient demand increases, the ABCC injects additional bias current, enhancing SR and improving dynamic behavior. Under steady-state conditions, the bias returns to its nominal low-power value.

2.2 | Simulation Setup

Circuit simulations were performed using HSPICE under 0.18 μm and 90 nm CMOS technologies. The complete circuit schematics implemented in 0.18 μm and 90 nm CMOS technologies are illustrated in *Figs. 2* and *3*, respectively. These figures present the full transistor-level design along with device dimensions, enabling a direct comparison of structural implementation and sizing strategies across the two technology nodes. The supply voltage was 3 V, and the amplifier operated in subthreshold region for low-power operation [18]. Simulation conditions are shown in *Table 1*:

Table 1. Simulation conditions.

Input Signal	Pulse Waveform
Amplitude	0.5–1.3 Vpp
Frequency	1 kHz
Bias current	50 nA
Compensation capacitors	1 pF
Load capacitor	1 pF

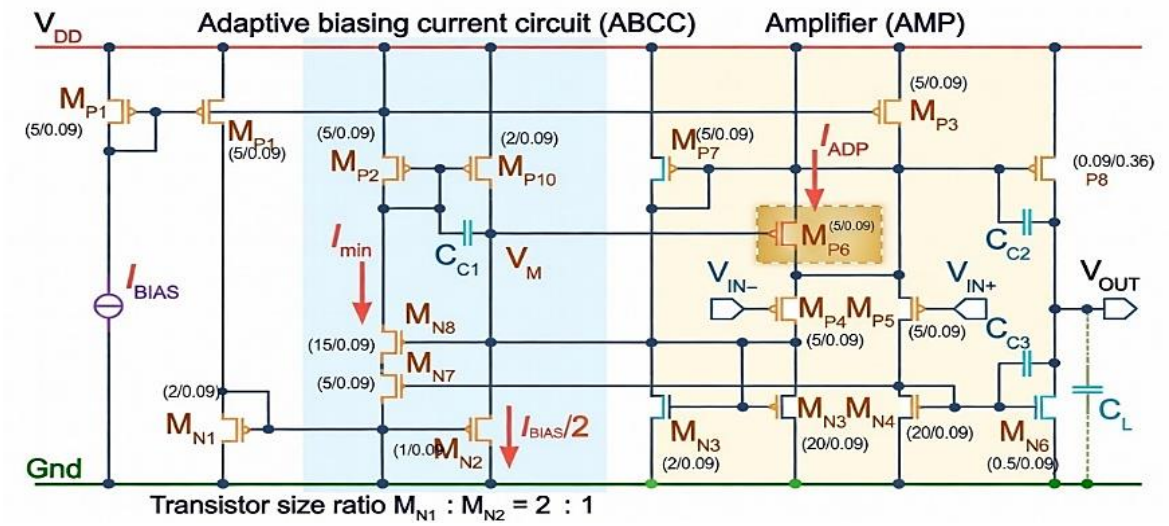

Fig. 2. Transistor-level schematic of the proposed amplifier in 90-nm CMOS technology with optimized device sizing parameters.

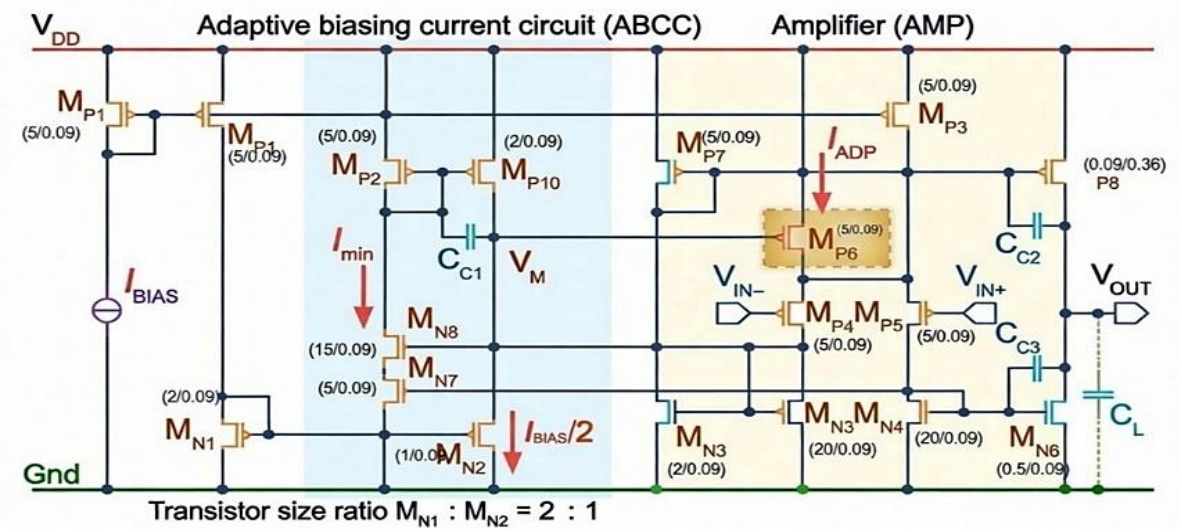

Fig. 3. Transistor-level schematic of the proposed amplifier in 0.18 µm CMOS technology with optimized device sizing parameters.

In order to evaluate the effectiveness of the proposed adaptive biasing strategy, two amplifier configurations were systematically analyzed: 1) the amplifier incorporating the ABCC, and 2) the conventional amplifier without the ABCC block. Both structures were implemented under identical biasing and process conditions to ensure a fair comparison. Key performance metrics were extracted from post-simulation analyses, including DC voltage gain, phase margin, positive and negative SRs (SR^+ and SR^-), total power consumption, and Bode plot characteristics. The DC gain and phase margin were obtained from AC small-signal analysis, while SR values were determined through transient simulations under large-signal excitation. Total power consumption was calculated from steady-state bias currents, and frequency response behavior including gain bandwidth and stability margins was evaluated using Bode plot analysis. This comparative methodology enables a comprehensive assessment of the ABCC's impact on stability enhancement, dynamic performance improvement, and power-efficiency trade-offs.

3 | Discussion

3.1 | Slew Rate Performance

SR was calculated using the 10%–90% method from the output pulse waveform. Results are summarized below:

Table. 2. Slew rate performance.

Technology	Total Current (nA)	SR− (V/µs)	SR+ (V/µs)
0.18 µm	132.198	0.25	0.20
90 nm	280.763	0.43	0.32

The 90 nm implementation demonstrates significantly higher SR due to improved transconductance efficiency and reduced channel length. However, this improvement is accompanied by increased total current consumption. The adaptive biasing mechanism enhances SR during transitions by temporarily increasing bias current, while preserving low static power in steady-state operation.

3.2 | Gain and Phase Margin

The Bode analysis demonstrates a clear performance enhancement when the ABCC block is incorporated, particularly in the scaled 90 nm technology. For the 0.18 μm implementation with ABCC, the amplifier achieves a DC gain of approximately 40 dB and a phase margin of about 62°, indicating stable closed loop operation with acceptable robustness. In contrast, the 90 nm design with ABCC exhibits a substantially higher DC gain of nearly 80 dB and an improved phase margin of approximately 85°, reflecting stronger loop stability and superior frequency compensation. This improvement can be attributed to the adaptive biasing mechanism, which dynamically adjusts branch currents and enhances effective transconductance during operation. When the ABCC block is removed, stability degrades significantly in the scaled technology node. Although the 0.18 μm amplifier without ABCC maintains a phase margin close to 60°, the 90 nm version becomes unstable, exhibiting a negative phase margin of approximately 70°. This result confirms that technology scaling intensifies parasitic effects and pole shifting, making adaptive biasing essential for maintaining stability. Overall, the results verify that the ABCC architecture not only enhances gain but also plays a critical role in ensuring robust loop stability, especially in deep submicron implementations. These gain and stability analyses are illustrated in Figures 4 and 5, respectively, in the form of Bode plots. The negative phase margin in the 90 nm configuration indicates severe instability when ABCC is removed. This confirms that the adaptive biasing circuit is essential for maintaining loop compensation and stability.

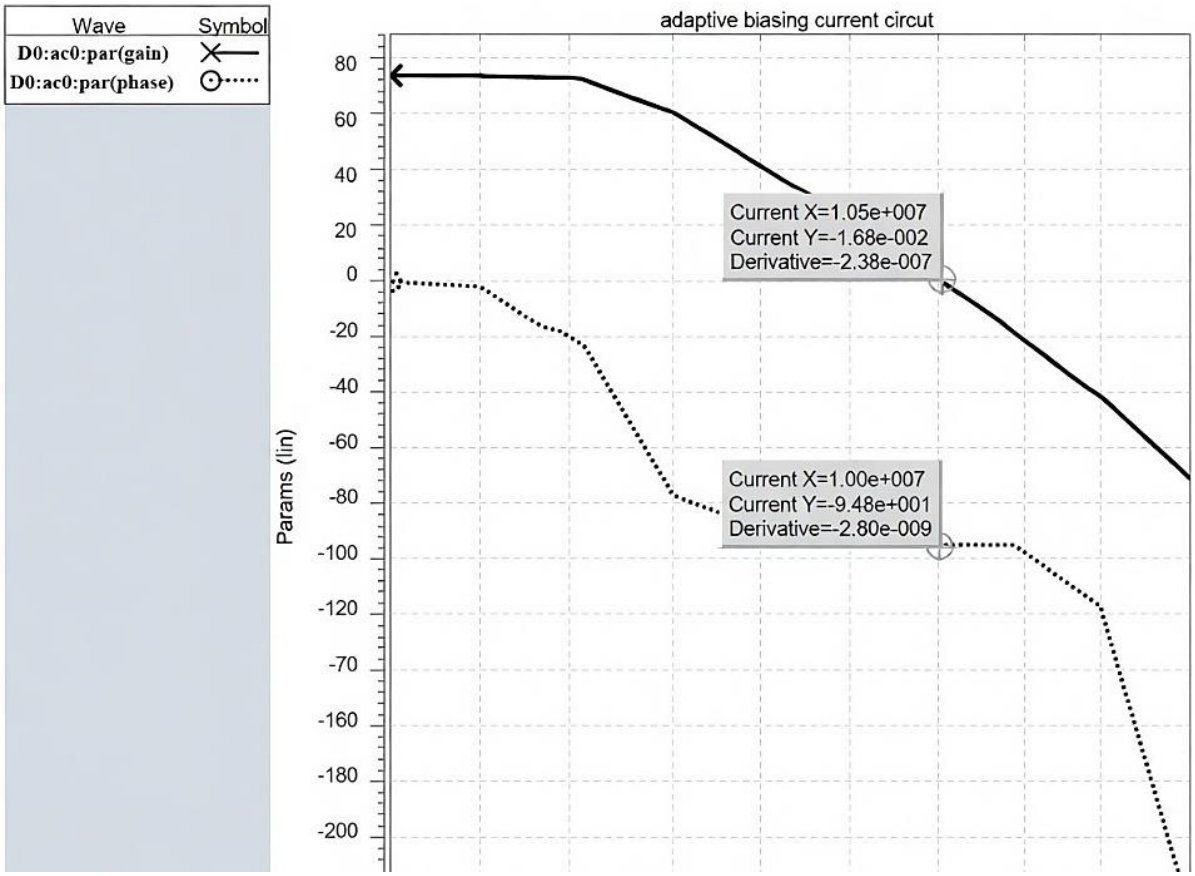

Fig. 4. Transistor-level schematic of the proposed amplifier implemented in 90 nm CMOS technology, including detailed device dimensions (W/L ratios).

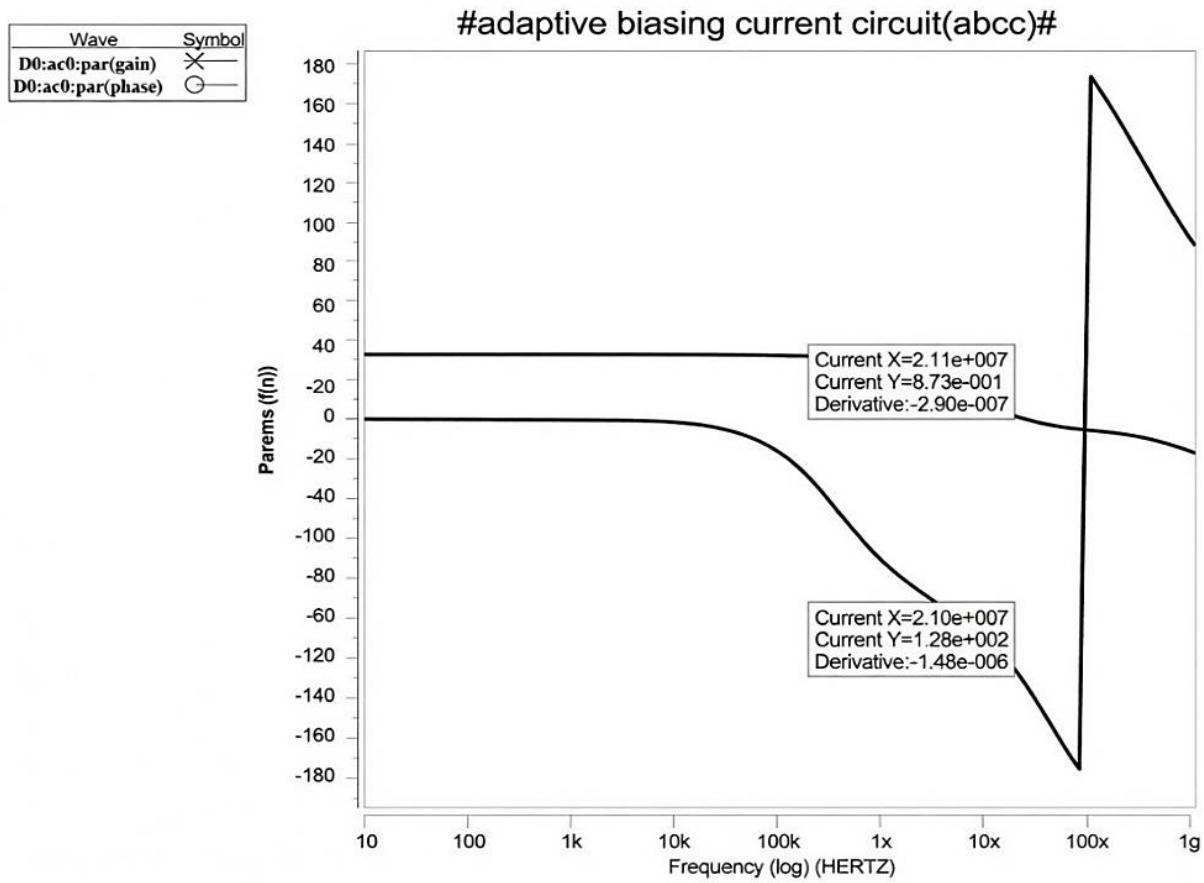

Fig. 5. Bode plot of the proposed amplifier implemented in 0.18-µm CMOS technology, illustrating the magnitude and phase responses obtained from AC small-signal analysis

3.3 | Simulation and Analysis of the Amplifier Without the ABCC Block

To evaluate the impact of the ABCC block on circuit performance, the amplifier was simulated after removing the ABCC structure. The results indicate that although certain parameters, such as the small-signal voltage gain, exhibit an apparent increase, the overall dynamic behavior of the circuit degrades significantly. In particular, the amplifier demonstrates severe instability and fails to operate reliably under typical operating conditions. As illustrated in *Figs. 6* and *7*, the absence of the ABCC block leads to improper frequency compensation and unfavorable pole–zero shifting, which ultimately compromises loop stability. This degradation becomes more pronounced in scaled technologies. For instance, simulations performed in 90-nm technology reveal that the SR is substantially reduced, indicating poor large-signal performance and limited transient response capability. These findings confirm that despite minor improvements in certain static parameters, the removal of the ABCC block results in critical stability and dynamic performance issues, underscoring its essential role in ensuring robust and reliable amplifier operation.

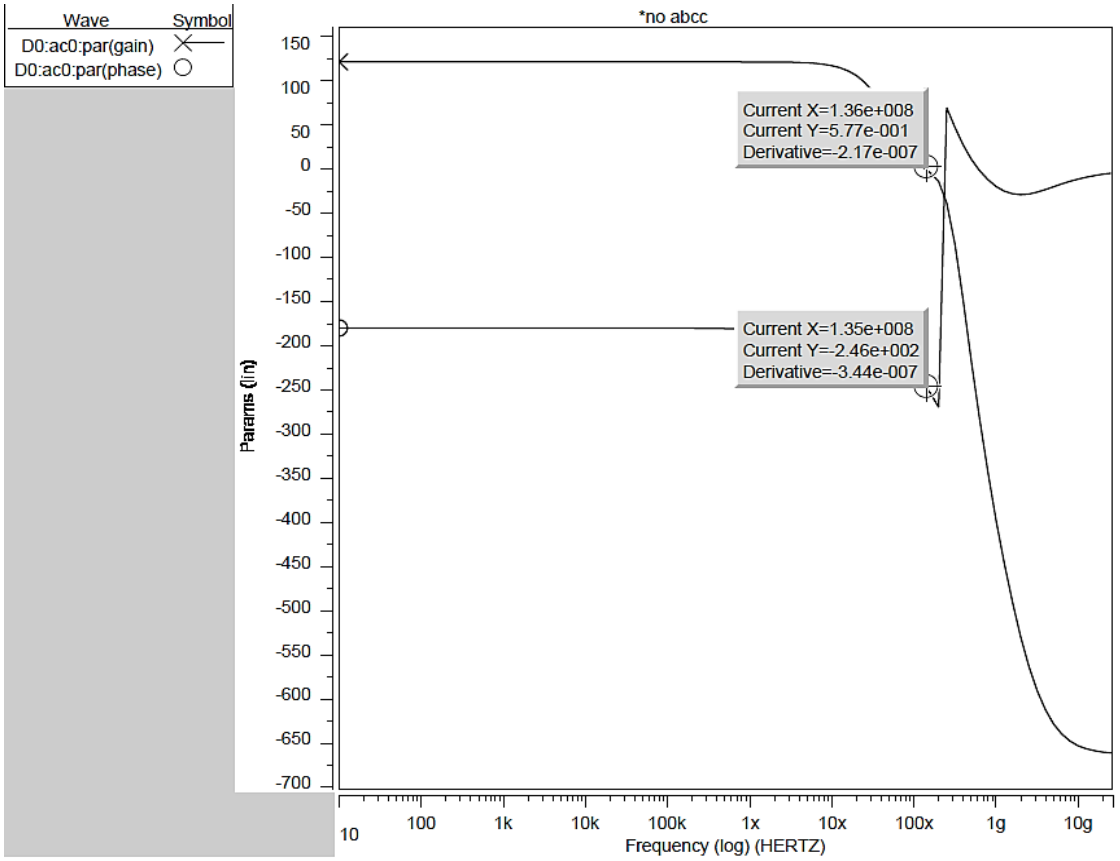

Fig. 6. Phase margin and gain curves of the amplifier without the ABCC block in 0.18-µm technology.

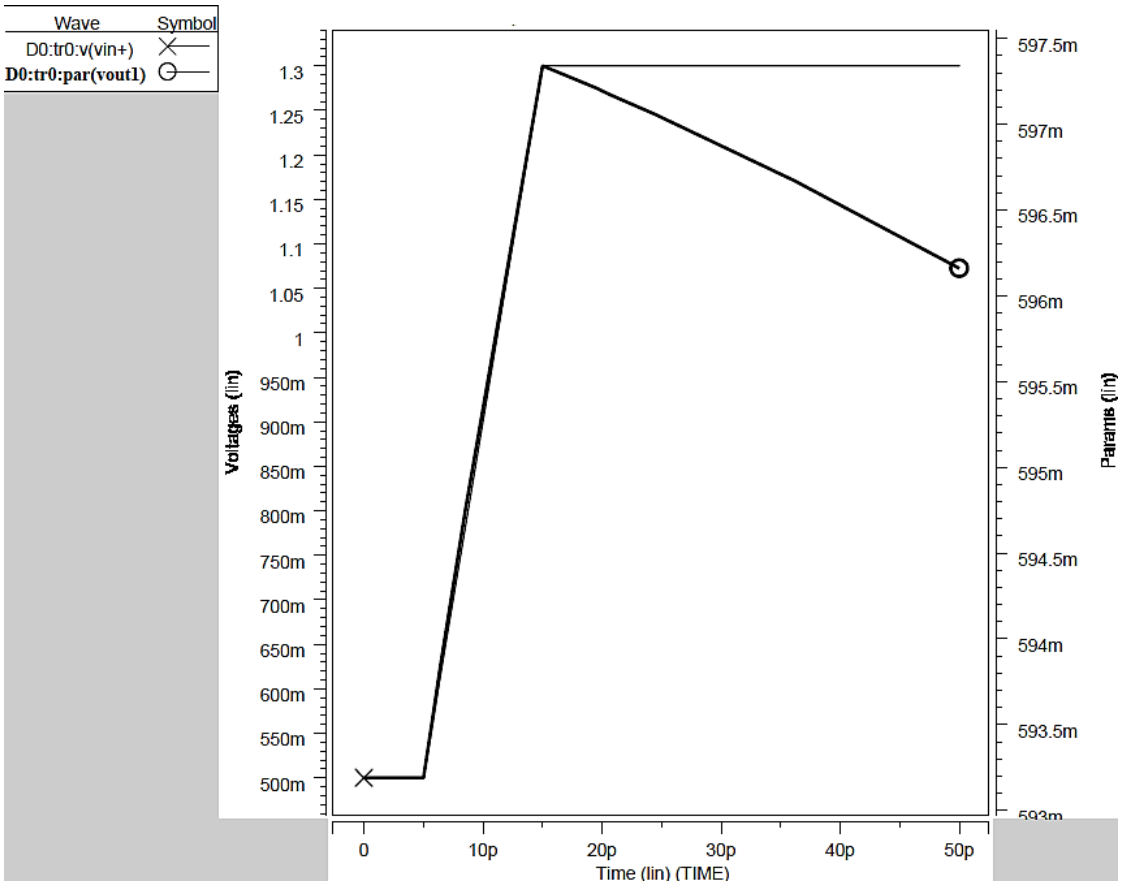

Fig. 7. Slew rate (SR) curve of the amplifier without the ABCC block in 0.18-µm technology.

3.3 | Power Consumption Trade-Off

The power comparison indicates that, while removing the ABCC block results in a reduction of static power consumption as shown in *Table 3*, it also introduces significant drawbacks, including circuit instability and degraded transient response. Consequently, the slight increase in power consumption associated with the inclusion of the ABCC block is justified, as it provides substantial improvements in overall circuit performance, notably enhancing stability, phase margin, SR, and convergence behavior.

Table. 3. Power consumption trade-off.

Configuration	Technology	Power
With ABCC	0.18 μm	466 μW
With ABCC	90 nm	233 μW
Without ABCC	0.18 μm	161 μW
Without ABCC	90 nm	98 μW

3.4 | Overall Discussion

The results demonstrate that:

I. The adaptive biasing mechanism significantly improves transient performance.

II. The 90 nm technology achieves higher gain and phase margin due to improved intrinsic device parameters.

III. Stability degrades drastically without ABCC, especially in scaled technology nodes.

IV. The trade-off between power and performance is optimized when ABCC is retained.

From a biomedical implant perspective, stability and predictable transient response are more critical than minimal static power. Therefore, the proposed adaptive amplifier with ABCC in 90 nm technology represents the best compromise between power efficiency and robust operation. Comparison of the parameters obtained from the amplifier circuit simulation in 0.18 μm and 90 nm technologies, for both configurations with and without the ABCC block is illustrated in *Table 4*.

Table 4. Comparison of the parameters with and without the ABCC.

Phase Margin (°)	Gain (dB)	Power Consumption (mW)	Technology	Configuration
62	40	466	0.18 μm	Amplifier with ABCC
85	80	233	90 nm	Amplifier with ABCC
60	40	161	0.18 μm	Amplifier without ABCC
-70	125	98	90 nm	Amplifier without ABCC

4 | Conclusion

In this study, the design and simulation of a low-power operational amplifier with and without the ABCC block were investigated in 0.18 μm and 90 nm technologies. Simulation results demonstrated that incorporating the ABCC block, despite a slight increase in power consumption, significantly improves circuit stability, phase margin, SR, and overall convergence behavior. Notably, the 90 nm design with ABCC exhibited superior performance in terms of gain and phase margin compared to other configurations, while removing the ABCC block resulted in severe instability and degraded transient response. Therefore, it can be concluded that integrating the ABCC block is an effective strategy for optimizing the performance of low-power amplifiers with high stability, and employing advanced technology (90 nm) provides additional

advantages in gain and dynamic response. These findings are particularly relevant for the design of low-power amplifiers in sensitive applications, such as implantable medical devices.

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Data Availability

The dataset analyzed in this research was obtained through survey responses and processed using PLS-based structural equation modeling techniques. Access to the dataset may be granted upon reasonable request to the corresponding author.

Conflicts of Interest

The authors report no competing interests that could have influenced the outcomes of this research.

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